Abstract

A transient rejecting system for protecting the state of a memory is described. The transient rejecting system includes a signal transfer circuit and a charge storage circuit coupled to at least one pin of a circuit. The signal transfer circuit receives a supply signal and determines when a transient event occurs. When a transient event occurs, the charge storage circuit provides a signal to the pin of the circuit maintaining the state of the memory prior to the transient. During normal operation, the charge storage circuit is charged, and the supply signal is provided to the pin of the memory circuit. P-channel FETs are used in the signal transfer circuit and allow for low voltage operation of the transient rejecting system.